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09/823,602	03/30/2001	Joseph Jeddeloh	MIC-4	6053
1473 7590 06/26/2008 ROPES & GRAY LLP PATENT DOCKETING 39/361 1211 AVENUE OF THE AMERICAS NEW YORK, NY 10036-8704			EXAMINER CHEN, TSE W	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

1. Applicant's arguments filed June 12, 2008 have been fully considered but they are not persuasive. Applicant argues that the references do not teach "accessing a look-up table..." Examiner disagrees and submits that the references teach each and every limitation of the claim, including the elements of a plurality of memory clock frequencies each associated with a number and a type of memory modules [see rejection of claim 1]. One with ordinary skill in the art would know that tables, as shown by Hartwell [tables 1-4] and Stevens [table 1], organize data containing associations between elements. Since the references teach the concept of organizing data in some form, it would have been obvious to one of ordinary skill in the art to substitute one form [e.g., look-up table] for the other [e.g., graph] to achieve the predictable result of data containing a plurality of memory clock frequencies each associated with a number and a type. As such, Applicant's arguments are deemed not persuasive and the rejections are respectfully maintained.